Enabling Systems for Use with the AMD SPIKE™ Debug Interface

Application Note

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The AMD SPIKE™ debug interface connects to a system motherboard via a connector using the low pin count (LPC) interface. The connector used for the AMD SPIKE interface has physical and electrical requirements described in this application note.

OVERVIEW

The AMD SPIKE™ interface is a development and debug interface for legacy-free PC systems, such as the AMD EasyNow!™ reference platform.

Legacy-free PC systems omit the RS-232 serial ports and ISA-bus LED display ports traditionally used to help debug and develop BIOS and operating system software. Some legacy-free systems also omit PCI slots, and the included USB or IEEE 1394 interfaces are not suitable for low-level debugging because of their internal complexity.

The AMD SPIKE interface solves this problem, providing a simple debugging interface with the following features:

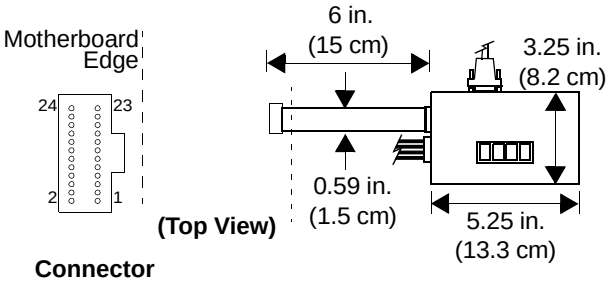
- A simple RS-232 serial port
- Two byte-wide hexadecimal LED displays
- Four software-defined configuration DIP switches
- A Reset button
- An Interrupt button
- Independent power input

For details about using the AMD SPIKE interface, see the *AMD SPIKE Debug Interface User's Manual*, order #23437.

PHYSICAL REQUIREMENTS

The AMD SPIKE interface connects to the low pin count (LPC) interface found in all modern chipsets. The AMD SPIKE interface requires a keyed 24-pin header, type AMP 1-104068-1 or equivalent. For easy access, this header should be located near the edge of the host system motherboard. Also avoid placing high-profile components between the connector and the board edge, where they might interfere with or damage the AMD SPIKE interface's ribbon cable.

To help determine the most convenient connector placement, Figure 1 shows the proper orientation of the connector with respect to the board edge, as well as the dimensions and typical orientation of the AMD SPIKE interface and its host connection cable.



Notes:

Allow 0.1 inch (2.5 mm) clearance around motherboard connector. Avoid placing high-profile components between the connector and motherboard edge.

Figure 1. Orientation and Dimensions

CONNECTOR SCHEMATIC

Figure 2 shows a typical host motherboard connector schematic for use with the AMD SPIKE interface. Connector signals are described in the following section.

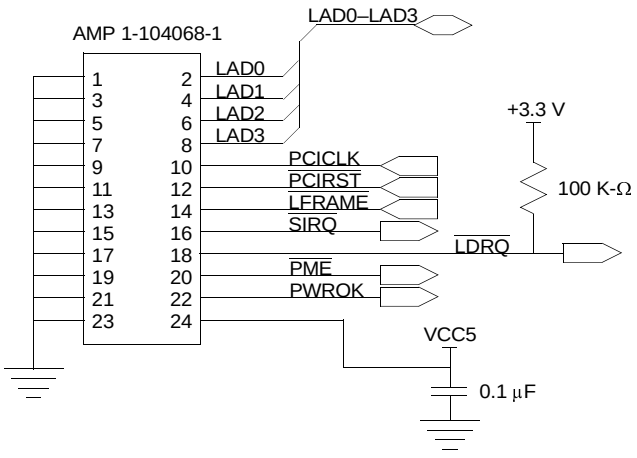


Figure 2. Motherboard Connector Schematic

Publication# **23702** Rev: **A** Amendment/**0**
Issue Date: **March 2000**

CONNECTOR SIGNAL DESCRIPTIONS

The LPC interface standard provides support for simple non-PCI devices in legacy-free systems. To reduce pin count and cost, the LPC interface transfers serialized data over a four-bit bus. For details about the LPC protocol, see the *Low Pin Count (LPC) Interface Specification, Revision 1.0*, available from **www.intel.com**.

The following sections briefly describe the LPC signals used to implement the AMD SPIKE interface connector on the host motherboard. Note that some chipsets might not implement all LPC signals. Also, the AMD SPIKE interface PWROK and VCC5 signals are not defined by the LPC specification.

LAD0–LAD3

These 3.3-V bidirectional signals carry multiplexed commands, addresses, and data to and from the peripheral.

If not provided within the chipset, each of the LAD0–LAD3 signals requires a weak (approximately 100 K-Ω) pullup resistor to hold the signal High during the second clock of a turn-around (TAR) cycle. See the LPC specification for details.

$\overline{\text{LDRQ}}$

This 3.3-V host input carries encoded DMA/bus master requests from the attached peripheral to the host. A separate $\overline{\text{LDRQ}}$ signal is used for each peripheral.

The $\overline{\text{LDRQ}}$ signal should be equipped with a 100 K-Ω pullup resistor to prevent spurious requests.

$\overline{\text{LFRAME}}$

This 3.3-V host output is pulsed Low by the host to indicate the start of an LPC cycle, or held Low to indicate an aborted cycle.

PCICLK

This is the host's 3.3-V, 33-MHz clock output, used to synchronize LPC cycles. This signal is typically derived from, and has the same phase and skew characteristics, as the system's PCI bus clock. This signal is named LCLK in the LPC specification.

$\overline{\text{PCIRST}}$

This is the 3.3-V system reset for both the AMD SPIKE interface and the host. This signal is typically the same as the PCI bus reset signal. This signal is named $\overline{\text{LRESET}}$ in the LPC specification.

$\overline{\text{PME}}$

This 3.3-V host input is the PCI Power management signal used by the peripheral to request wake-up from a low-power state.

PWROK

This 5-V signal is not defined in the LPC specification. It is connected to the host's power good signal. This allows the user to reset both the AMD SPIKE interface and the host by pressing the Reset button on the AMD SPIKE interface.

This signal is *not* the same as the LPC's $\overline{\text{LPCPD}}$ signal, which is not used by the AMD SPIKE interface.

SIRQ

This 3.3-V host input is used by the peripheral to issue serialized interrupt requests to the host. This signal is named SERIRQ in the LPC specification.

VCC5

This 5-V host output is not defined in the LPC specification. The AMD SPIKE interface uses this signal to sense that a host is attached and powered. The AMD SPIKE interface places a 20 mA load on this signal.

Note: *The LPC signals are not buffered in the AMD SPIKE interface. Always apply power to the AMD SPIKE interface before applying power to the host. Powering the host first can irreparably damage the AMD SPIKE interface.*